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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/325,882	06/04/1999	DAVID E. SINCLAIR	0100.9900390	3412

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EXAMINER
KIM, HAROLD J

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 10/09/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/325,882	SINCLAIR ET AL.	
	Examiner	Art Unit	
	Harold Kim	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *9/12/02* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This Office Action is in response to the filing of the Amendment B, Paper # 10, on 9/12/02, has been considered but the arguments are moot in view of the new ground(s) of rejection.

2. Claims 1-19 are presented for examination.

3. Jones, Jr. and Houston were cited in previous office action.

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. **Claims 1, 4, and 7 rejected under 35 U.S.C. 102(e) as being Lin by US Patent no. 6,256,746.**

6. In re claim 1, Lin shows a power consumption reduction circuit [fig 4] comprising:

a memory clock source [104, figs 4]; and

a memory clock tree circuit [116, fig 4], operatively coupled to the memory clock source, that generates branches of memory clock output signals as a plurality of corresponding independent clock signals [404, 408, 412 and 416, fig 4] to a number of memory interface circuit [406, 410, 414 and 418] for differing processing engines and selectively activates at least some of the plurality of independent clock signals in response to received condition data [606, fig 6] during an active mode [last four lines of Abstract].

The limitation "for a graphic controller" has no patentable weight since it is intended use. It has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex parte Masham, 2 USPQ2d 1647 (1987).

7. In re claim 4, Lin shows a plurality of memory read latch circuits [504, 510, fig 5] and a memory read latch control circuit [116, fig 5].

8. In re claim 7, Lin shows the memory clock tree circuit includes a plurality of logic circuits [406, 410, fig 4], wherein each logic circuits outputs one of the plurality of corresponding independent clock signals [404, 408, fig 4] and wherein each logic circuit is coupled to operatively receive different condition data associated with different condition data sources [fig 6].

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to

a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

11. Claims 2, and 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin, US Patent no. 6,256,743.

12. In re claims 2, and 17-19, Lin shows an engine clock source [104, fig 4] operatively coupled to a switching circuit [116, fig 4] that generates an output clock signal [404 in fig 4] that is selectively coupled as a clock signal [404 in fig 4] to a functional unit [406] including graphics [col 11, line 37] such that the switching circuit disables the output clock signal based on standby mode data [col 11, lines 7-29].

Lin does not show the function unit as a video overlay engine, a video capture engine, I2C control logic and a multimedia port, and the received condition data as video capture data. However, it is well known in the art of computer system to have the video overlay engine, the video capture engine, I2C control logic, a multimedia port, and video capture enable data. Therefore, Lin does not need to specifically the video overlay engine, the video capture engine, the I2C control logic, the multimedia port and the received condition data as video capture enable data since one skilled in the art at the time of invention is presumed to know something about the art apart from what the reference literally disclose. *In re Jacoby*, 309 F.2d 513, 135 USPQ 317 (CCPA 1962).

It is also well settled that obviousness may be concluded from common knowledge and common sense of the person skilled in the art without a specific hint or suggestion. *In re Bozek*, 416 F.2d 1385, 163 USPQ 545 (CCPA 1969).

13. **Claims 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin, US Patent no. 6,256,743 in view of Jones, Jr., US Patent no. 5,781,768.**

14. In re claim 3, Lin does not show a variable memory clock control circuit operative to vary a speed of the memory clock based on a type of memory request from a plurality of memory requestors. However, Jones, Jr. shows a variable memory clock control circuit [4, fig 4] operative to vary a speed of the memory clock based on type of memory request from a plurality of memory requestors [col 3,lines 8-66].

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the variable memory clock control circuit operative to vary a speed of the memory clock based on type of memory request from a plurality of memory requestors as shown in Jones, Jr. for reducing the power consumption by lowering the clock frequency.

15. Claims 5-6, and 8-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin, US Patent no. 6,256,743, in view of Jones, Jr., US Patent no. 5,781,768, and in further view of Houston, US Patent no. 5,544,101.

16. In re claims 5-6, Lin shows the memory read latch circuit generates a read latch enable signal [402 in fig 4; 508, fig 5], a gating circuit [AND gate in fig 4] responsive to the read latch control signal [402 in fig 4] and a memory clock signal [302 in fig 4] operative to selectively enable and disable memory read latches [504, 510 in fig 5] as a

function of memory requests. The combination of Lin and Jones, Jr. does not show a read data latency compensation circuit, a multiplexer having a output operatively coupled to the gating circuit, a first input coupled to receive the memory clock signal, and a second input coupled to receive a memory clock feedback signal wherein the multiplexer is controlled to output the memory clock signal.

Houston shows a read data latency compensation circuit, a multiplexer having a output operatively coupled to the gating circuit, a first input coupled to receive the memory clock signal, and a second input coupled to receive a memory clock feedback signal wherein the multiplexer is controlled to output the memory clock signal [fig 1].

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a read data latency compensation circuit, a multiplexer having a output operatively coupled to the gating circuit, a first input coupled to receive the memory clock signal, and a second input coupled to receive a memory clock feedback signal wherein the multiplexer is controlled to output the memory clock signal as shown in Houston to the combination for a memory device to consume as little power as possible [Houston, col 2, lines 34-36].

17. Claims 8-16 are rejected under the same rationale as discussed above in claims 1-7.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Further references of interest are cited on Form PLO-892, which is attachment to this office action.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 746-7239 for regular communications (for informal or draft communications, please label "PROPOSED" or "DRAFT"), and

(703) 746-7238 for After Final communications.

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Fourth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application should be directed to the technology center receptionist whose telephone number is (703) 306-5631.

Direct any inquiries concerning drawing review to the Drawing Review Branch (703) 305-8404.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Harold Kim whose telephone number is (703) 305-1948. The examiner can normally be reached on Monday-Thursday 6 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey Gaffin can be reached on (703) 308-3301.

Harold J. Kim
Patent Examiner
October 6, 2002/HK

JEFFREY GAFFIN
SUPERVISORY PATENT EXAMINER
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